Hole Plugging Technology for High Density Circuitry and Conventional Through Hole Multilayer PWBs

by **MICHAEL CARANO**

INTRODUCTION

Filling of plated through holes is not new to the PWB fabrication industry. For many years, end users required some or all via holes to be partially plugged with solder mask. This task was required in order to prevent solder from wicking through the holes (to the component side) during the assembly process, and to create a vacuum for electrical test. Minimizing flux residues in the holes is another valid reason to undertake this operation.

The concern of plugging through holes with a standard LPI resides in the fact that these inks are typically 60–80% solids content. During the drying/curing process, the solvent evaporates and the hole plug shrinks, often leaving a small gap between the through hole barrel and the plug. This, of course, can lead to a lack of adhesion of the plug to the hole wall. There is a second risk: residual solvents from the LPI. During the curing process, operating conditions may lead to a "skinning over" of the plug. This scenario causes solvent to remain entrapped within the hole. The consequence is the solvent will expand during the heat of the soldering operations, leading to cracking of the fill. As through hole aspect ratios increase, it may become impossible to evacuate all of the solvent. Process curing temperatures and ramp-up time to cure must be carefully monitored, regardless of the technology level of the PWB. This issue will be presented in detail elsewhere in this article.

While many fabricators continue to be somewhat successful with conventional plugging with LPIs, the growing density and miniaturization of complex electronic interconnection substrates requires new process technology. The LPIs have limitations that can only be addressed with the so-called plugging pastes. These plugging pastes are nearly 100% solids content, and were primarily developed for blind and buried vias and sequential build technology. However, other formulations have been developed for filling through holes in order to replace the LPI inks, based on the same principle of 100% solids content.

This article will review both the filling and plugging process, including the materials utilized, methods of application, and advantages and disadvantages of the plugging process.

DEFINITIONS

It is helpful to understand the term, "via hole plugging" versus "via hole filling." This is an important distinction, but nonetheless must be put in the proper perspective. Via hole filling is used for the non-planar filling of plated through holes. Via hole plugging is synonymous with the planarization of blind and buried vias. Via hole plugging is applicable to HDI and microvia designs. Brushing (or planarization) is required to remove the excess material and create the flat surface. This technique will be discussed in the section on " The Process of Via Hole Plugging."

Via hole plugging is in demand due to the explosive growth in HDI designs employing area array for IC packaging, via in pad, and landless designs. Achieving planarity of the via for dielectric formation is another key market driver. Uniform dielectric spacing between layers of circuitry and the ability to metallize the dielectric, as well as achieve plating adhesion, is critical.

In Figure 1, the construction describes an HDI substrate with both plated through holes, filled buried vias, and microvias. The plated through holes pass through the entire board, and do not require a planar and complete filling. A standard via hole fill would suffice. In this example, the substrate has a core that has been fabricated using conventional methods. The core has a dielectric layer on each side. Microvias have been formed connecting Layers 2 to Layer 3, and Layer n to Layer n-1. The top layer is then metallized, and a second dielectric layer applied to each side. Microvias are again formed to connect Layer 1 to Layer 2. A PTH is formed connecting all of the layers. It should be noted that this example includes a buried via connecting Layer 3 to Layer 4. The buried via is a candidate for hole plugging.

With respect to the blind vias, generally sufficient resin is available through the use of resin coated foils to fill the vias. This is only recommended for small diameter, blind vias that are low aspect ratio. Larger diameter

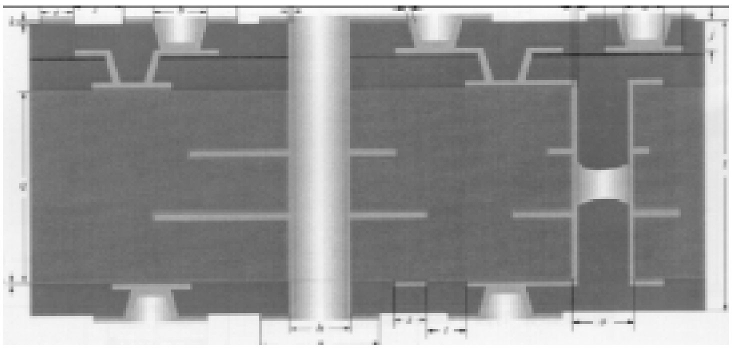


Figure 1. Examples of vias. (IPC Technology Roadmap-National Technology Roadmap for Electronic Interconnections 2000-2001.)

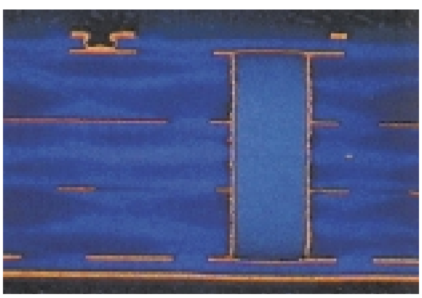


Figure 2. Buried via filled with a plugging type paste. Surface blind via can be filled with a standard hole fill.

blind vias or small diameter blind vias of high aspect ratios will not have sufficient resin available to fill the vias. Air inclusions during the lamination process may reduce long-term reliability. Possible alternatives are the utilization of liquid epoxy dielectrics or specially formulated plugging pastes.

When using liquid epoxy, plugging is sometimes ineffective due to insufficient flow of the resin into the holes. However, resin coated foils are utilized to fill blind vias, provided that the via diameters are not too large, and the via depth is not such that the resin forms an incomplete fill. Thicker core panels and/or higher aspect ratio vias will require a different via hole plugging technology.

In addition, there are other limitations to hole plugging with resin coated copper. The resin of the resin-coated foil has a relatively high coefficient of thermal expansion (CTE) of about 60 ppm below the glass transition temperature. This is typical of non-glass reinforced resin systems. Thermal excursions, such as thermal shock, will increase the load on a via and cause cracks or delamination in the fill. This is primarily the result of different CTEs between the various materials exacerbated by any air inclusions.

Attempting to fill larger volume holes, as an example, with thicker panels, can lead to pitting because of the quantity of resin material available for filling is insufficient.

BURIED VIAS

Figure 2 shows the typical candidate for via hole plugging. The buried via has a very large volume to fill, and the requirement for complete fill with a planar surface is necessary in order to form the next dielectric layer.

HOLE PLUGGING-REQUIREMENTS AND GENERAL PROPERTIES

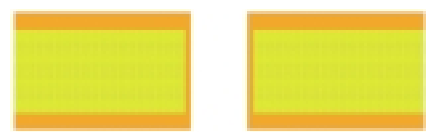
Plugging pastes required for filling buried vias are nearly 100% solids content with a low CTE of <40 ppm. This requirement is needed in order to prevent cracking or delamination after a thermal excursion. Pencil hardness of this type of plugging paste is in the range of 6-8 H. The hole plugging requirements are summarized below:

- No air inside the paste
- Flat surface after plugging; no sagging
- Good adhesion of the paste to the copper in the via
- Relatively easy to metalize the cured paste in subsequent operations
- Good adhesion of photoresist and dielectric
- Tg > 140 °C
- CTE < 50 ppm (below Tg)
- Easy to brush without risk of removing paste leading to a dip in the plug

PROCESS FLOW FOR HOLE PLUGGING

Step 1: Surface Preparation

The process flow for via hole plugging is shown stepwise below. It is assumed that the buried via layer has been fabricated, with vias formed and metalized. At this point, the via is prepared for plugging through a series of cleaning steps designed to remove oxides and mirco-roughen the copper in the via to enhance adhesion of the plugging paste. It is common practice to treat the surface and holes with an oxidizing solution, such as a conventional black or brown oxide. The oxide coating with its high surface area due to copper oxide crystal growth, enhances the bond between the plugging ink and the via.

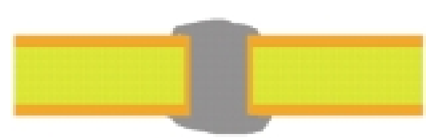


Step 1.

Step 2: Plugging Via

The second step requires that the via be filled with the plugging paste. Generally, two options are available for this operation:

- Roller coating process
  Screen printing process



Step 2.

ROLLER CO ATING

Plugging vias with the roller coating technique requires investment in capital equipment. Forcing the paste through the vias by means of a roller effects the plugging operation. Paste is held in a trough and the action of the roller picks up the paste on the underside of the roller. The PWB is pressed against the coating roller from above, and the paste that is located between the PWB and the roller is pressed through the vias. The board then passes through squeegees designed to remove excess paste.

The advantages and disadvantages of the roller coating process is detailed below.

Advantages:

- Rapid filling of vias
- No screen stencils required
- Ease of planarization due to relative cleanliness of surface
- Fewer process parameters to control versus screen process

Disadvantages:

- Vias not required to be plugged must be masked off
- Higher risk of dip formation in the plug
- Trough volume of 8–10 kgs required (paste must have good shelf life)

The issue with the risk of dip formation has to do with the flow characteristics of roller coating formulations. These particular pastes, applicable to roller coating, possess certain flow characteristics. These flow characteristics are related to capillary effects, i.e., the smaller the hole diameter, the greater the dip. Newer formulations have been developed that have had their curing characteristics modified to eliminate this potential for sagging.

SCREEN PRINTING

This process employs a stencil with the via pattern drilled to match the pattern of vias on the PWB. Screen printing requires that the vias be completely filled with one stroke of the squeegee. Otherwise, air will be entrapped within the plugging paste.

One particular requirement for the screening process is that ink should protrude equally from both sides of the via. This requirement is met by placing a backup board (a stencil drilled with the same hole pattern) underneath the PWB. This allows the paste to fill the via. A small nail head is formed on the underside, ensuring a complete fill.

Of course, unlike the roller coating process where few operating parameters were considered critical, screen plugging of inks is a different matter. Screen mesh, screen tension, squeegee profile (rounded or right angled), off contact, and squeegee hardness affect the quality of the fill. A manufacturer must make adjustments in these process parameters depending on via aspect ratio. Often, several test panels must be processed in order to dial in the process.

Advantages:

- Vias not requiring fill are kept free of plugging ink
- Well known and easy to control process
- Wide availability of screen printing equipment

Disadvantage:

- Screen stencil required for each layout
- Some difficulty printing designs with significantly varying hole diameters

CURING OF THE PLUGGING PASTE AND PLANARIZATION

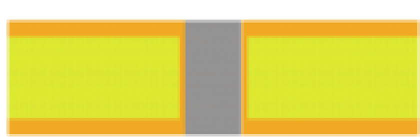
Once the paste has been applied to the vias, the via hole plugging material must be cured. There are both thermal curing and UV curing versions of plugging pastes commercially available.

Thermal curing requires a temperature of approximately 150˚C for 30–45 minutes, depending on the particular product used. The thermal curing version is single stage. However, with this version, one must be careful not to over-brush the PWB. Overbrushing will remove plugging paste from the via, causing a loss of planarity. The use of brushes with a ceramic surface give very good results. The formation of the nail head (mentioned above) is beneficial in providing sufficient material in the plug so as not to create the "dip."

Step 3: Curing and Planarization

UV curing formulations are pre-hardened under the influence of UV light. The hardness of the plug at this stage is 2H-3H. This will facilitate the brushing or planarization of the excess material, rendering a flat or planar surface. Then, in this two-step curing process, the PWB is given a final cure with IR to increase the hardness to approximately 8H. The UV formulations are generally two-part systems.

For planarization to be deemed successful, complete removal of the protruding ink, while not removing any of the material from the via, is required. The brushing process must not damage the knee of any unplugged holes, and copper should only be removed evenly and minimally along with the excess plugged material. Brushing equipment should be equipped with a very precise and fast pressure control system, as well as an automatic system for measuring panel thickness.



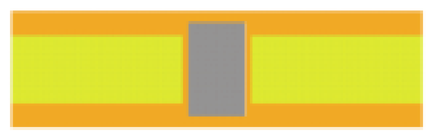
Step 3.

The brushing or polishing step must provide a level surface and as smooth as possible. Uneven surface must be avoided. Soft brushes must not be used over concerns of causing the excess removal of the plugging paste. The UV hole plugging processes must then receive a final cure to increase the hardness and advance the final properties of the plugging paste. The thermal-cure-only process is ready for brushing after the thermal excursion.

Once this is complete, the buried via layer is ready to be processed for metalization with conventional technologies. These processes are well documented and will not be repeated here.

Step 4: Metalization

After the metalization step is complete, the buried via layer is ready for the remaining steps in the sequential build process.



Step 4.

LIMITATIONS OF HOLE PLUGGING

Reasonably, manufacturers should be able to completely fill vias with diameters between 0.1–2.0 mm. Of course, board thickness must be considered when making such a statement. As an example, one can expect that a board thickness of 1.5 mm with aspect ratios of 1:1 up to 10:1 be filled. Thinner boards may have difficulty filling holes due to stability of the thinner board. And, as board thickness exceeds 2.1 mm, it becomes increasingly difficult to plug the vias completely. Always consult the supplier of both equipment and material, and by all means process test panels for optimization purposes.

VIA FILLING OF CONVENTIONAL MULTILAYER BOARDS

Different products and processes are employed for the filling of vias on multilayer boards. These products and processes are in contrast to the process of via hole plugging as described above. Depending on hole diameter and aspect ratio, the following process technologies can be used:

- Conventional two-pack solder resists with solids content of 60-80%

- Photoimageable type solder resists with solids content of 60-80%
- Specially formulated via hole fillers with solids content of 100%

These specially formulated via hole fillers have flow characteristics that enable the filling of via holes up to a diameter of 0.8 mm.

Two pack solder resists as a hole filling option appeals to many fabricators due to availability, and the fact that they can be made to work. Additionally, the color of the via fill will match the color of the solder resist. However, matching the color of the fill with the mask cosmetics should not be the main reason for choosing this option. Functionality and performance of the via hole fill should be the only considerations. When utilizing solder resist (standard two pack resists and liquid photoimageable resists), one must be able to navigate around the issue of (1) shrinkage of the fill during cure, and (2) residual solvents remaining. Since these types of materials contain 20–30% by weight solvents (60–80% solids content), some the actual volume of the fill must shrink during the curing process.

Solvent evacuation must be carried out in order to properly dry and cure the fill. Thus, there is volume loss in the fill. A worst case scenario leads to loss of adhesion between the fill and the hole wall, due to thermal stress from the assembly operation. Secondly, residual solvents remain in the hole filling ink. The higher the aspect ratio, the more difficult it is to evacuate all of the solvent. The thicker the ink layer, the more difficult it is to remove all of the solvent. The main cause of solvent entrapment is due to the "skinning over" of the outer-most layers of the ink. The skin described earlier acts as a barrier preventing solvent within the ink from evaporating. When this situation occurs, the solvent undergoes expansion leading to possible cracking of the filling. This situation typically occurs with the hole plugging inks that are cured in a one-step mode, where the curing temperature is ramped up immediately. One way to solve this problem is to use a step curing technique, described below.

Note

Dan Feinberg

Hole plugging is a process that has not received a lot of published attention even though it is one of the processes that is not as well understood as the more mainstream areas such as primary imaging and metalization. When discussing this issue with my colleague Mike Carano (who is also the co editor of an upcoming Board Authority), he happened to mention that he was working on such an article. At the very last minute he graciously offered to spend his summer weekend writing instead of playing golf. The result is this valuable and informative article.

STEP CURING

Multiple curing steps are recommended whenever photoimageable solder masks and conventional inks are used to fill vias. The step curing process is carried out with a lower temperature than indicated by the supplier for proper curing temperature. This lower temperature should allow most of the solvent to escape before the ink material begins to polymerize. A three-step cure is practiced as well. The three-step process requires a lower temperature (for example, 80°C for 30 minutes) for the first step. A second step follows with 120°C curing temperature for 30 minutes. The first step allows the ink to dry without cross-linking. The final cure is carried out at a temperature of 150°C for 60 minutes.

Certainly, the dual or three-step process is time consuming and leaves room for process variation. Fortunately, via hole fillers specially formulated for filling holes are commercially available. These are discussed below.

SPECIALLY FORMULATED VIA HOLE FILLERS

Processes suited for via hole filling are based on 100% solids. The high solids content eliminates the possibility of solvent expansion and via plug shrinkage. The high solids content process does not require thinning with solvent. Most commercially available via hole fillers of this type are simple one-pack systems, requiring minimal preparation. Since most of these formulations are based on epoxy, the CTE of the material closely matches the CTE range of the laminate. This is beneficial for adhesion of the fill to the hole, and overall stability during any form of thermal stress due to soldering or other thermal excursions.

The epoxy via hole fillers described here are highly thixotropic with specific flow properties. Joint curing of these epoxy based via hole fillers is possible with solder resists.

The via hole fillers are applied through a screen-defined stencil. Typically, the "openings" in the screen should be slightly larger than the hole diameters one is trying to fill. High stencil thickness is generally not necessary, as the ink must only be printed into the holes.

PROCESSING PARAMETERS

- The screen mesh should be 90–115 to allow for maximum flow
- Squeegee at shore hardness of 60 to 65 (45-degree angle with flat bottom)
- Screen tension: 18–20 newtons
- Slow print speed to allow for fill
- Fill screen mesh with ink before printing (flood the screen)
- Multiple passes may be required to fill holes
- Observe proper cure temperature and time
- Allow air to escape through bottom of panel on screening table-use a course screen mesh placed under the board

It may require multiple passes to fill vias 0.3 to 0.4 mm in diameter.

PWB fabricators apply via hole fillers in a joint processing sequence with the solder resist. In this case (via hole fillers and LPI), the panels are processed through the step of developing. Then the via hole filler is applied, and the final curing process of both the LPI and the via hole fill occurs simultaneously. A slightly different variation occurs when PWBs with conventional two-pack solder resists are used in place of LPI. In this case, the two-pack mask must first be printed on each side of the panel and tack dried. Then the epoxy based via hole filler is applied. Final cure of the mask and fill are then carried out.

LIMITATIONS OF VIA HOLE FILLERS

Depending on equipment and the skill of the operators, hole sizes in the range of 6–8 mils (0.15–0.20 mm) are expected to be filled. However, the resolution accuracy of these materials as circuit density increases will necessitate the need to commercialize a photoimageable hole fill.

THE CAVEATS

Beside some of the obvious problems that can arise with either via hole plugging or a via filling operation, each fabricator must carefully choose the chemistry and the method(s) of application. Understanding the end user's requirements for circuit density, aspect ratio, and board thickness will help the fabricator make the proper investments.

Nonetheless, successful via hole filling and plugging is somewhat dependent on the quality of the via. For example, poorly drilled and rough vias can increase the likelihood of causing air bubbles or an incomplete fill. Copper nodules may be pushed back into the via during the planarization step involved in the hole plugging process. Surface burrs on the copper can lead to similar problems.

THE FUTURE

The demands of the digital age will only require interconnect substrates with increasing complexity. However, the need for complexity will come with the price of very high density. PWBs will be lighter, smaller, and require a significant increase in routing density. This means many more applications for blind and buried vias, via-in-pad, and padless designs. Stacked vias of increasingly higher aspect ratios will become a major design feature in the HDI landscape.

If manufacturers are going to be competitive as key suppliers of electronic interconnect devices, then mastering fabrication of HDI substrates and chip packages will be necessary. Fortunately, methodology, processing equipment, chemical technologies, and expert technical guidance is available. Reliable and robust hole plugging and hole filling technologies are just one subset of competencies required to compete on the HDI platform. This subset does exist today and improvements in equipment and chemistry will advance the industry well into the future. ■

NOTE: For more information, see Carano's article, "Metalization Processes for Blind Vias," *The Board Authority*, July 2002, Vol. 2, No. 2, pg. 22.

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