Integrating High Density Interconnect Microvia Technology into the Multilayer Board Mainstream

Jim Paulus
AlliedSignal Laminate Systems, La Crosse, WI

Frank Polakovic
Electrochemicals Inc., Maple Plain, MN

Abstract

High Density Interconnect (HDI) technology is gaining recognition in the industry as a primary means to significant gains in miniaturization and performance. It is also known as Build-up Multilayer, or BUM. The PCB manufacturing infrastructure has accepted the challenge and is developing quickly to support BUM technology-based programs.

The selection process for materials and processes to fabricate redistribution layers, which are the functional feature of BUM, is still immature and dependent on several factors, including technical feasibility, performance, and fit to the application. Some OEM's may include on their drawings a specification for one of the many BUM systems on the market, but most fabricators will determine which process is best suited and select the optimum material based on cost and performance.

Much attention has been given to photodefineable dielectrics, but the most direct enabler to BUM capability appears to be the use of lasers for microvia drilling and resin coated foils such as AlliedSignal's RCC® for the redistribution layer. RCC usage provides the fabricator conventional processability while offering enhancements over other types of material. However, FR-4 buildup layers continue to attract interest due to low cost and UL recognition issues.

This paper addresses the utilization of RCC for redistribution layers compared with thin FR-4 buildup layers with regard to laser ablation, hole desmear, and metallization, including direct plating technology. The results of evaluations of microvias in RCC and FR-4 will be reviewed, including the status of reliability testing. Although drawings of HDI parts utilizing BUM are appearing off designers' tables, the pace of acceptance appears slow. Our paper is intended to increase BUM usage by increasing the fabricator's understanding of the processes needed to build metallized microvias and address questions on interconnect reliability by thermal testing.

Introduction

Printed Circuit Board manufacturers worldwide are in the process of installing the capability to fabricate Buildup Multilayer Boards (BUM). The number of candidate build-up technologies is staggering. The majority of fabricators will choose from several photo defined dielectric systems (PDD) and a group of processes in which vias are drilled by wet or dry procedures. Via drilling includes laser, plasma, mechanical, and similar techniques.

Both PDD and via drilling have a multitude of dielectric material choices within them. PDD includes dry film versus liquid resists. Via drilling includes resin coated foil, copper-clad laminates based on aramid, polyimide film, and FR-4.

In most cases, a PCB manufacturer will look for the ability to integrate HDI technology into his process with minimal capitalization and manpower. This has been particularly the case as shown by the early interest in plasma ablation. Many shops have a plasma unit working as a desmear or etchback system. If capability existed to also remove exposed dielectric to create a blind via, the expansion to HDI would have been a modest operational stretch. However, plasma has not shown the desired consistency of performance from machines specially designed for microvia ablation, and thus the early expectation that conventional plasma could be used has been quashed.

All shops have photo departments with highly refined photo-lithographic capabilities, but in spite of this installed base, PDD requires significant investment in equipment and upgraded sophistication in artwork control and image development. Additionally, metallization by additive plating processes are prone to difficulties in adhesion, defects, and productivity.

The path that provides significant overlap to existing fabrication capability is that of via drilling in a conventional dielectric layer that has been laminated to a substrate, either prefabricated or built simultaneously with the entire board. This is where the majority of development is occurring today.

Many shops have decided on the via drilling approach (noting that some of the major houses are also developing competencies in PDD to extend their marketability). The past 12-18 months have been spent understanding materials and process interactions. The material choice increasingly has narrowed to RCC and FR-4. The next hurdle is to mainstream fabrication of redistribution layers using RCC and FR-4 into a shop's process. The final enabler is to demonstrate that a microvia interconnection is as reliable or more so than a comparable plated through via, so that prospective OEM's are comfortable with the technology.

Our presentation deals with studying the fabrication steps needed for metallizing microvias drilled in RCC and FR-4 layers, and the process of measuring their reliability using industry accepted thermal stress and thermal cycling techniques.

Microvia Drilling Process

A large segment of board shops interested in HDI have indicated a preference for laser usage. Lasers provide a low-threshold avenue to adding microvia drilling capability into a shop's process. The initial cost is roughly $400K per machine, for either UV-YAG or TEA-CO_2 lasers. The speed attainable is not comparable to PDD or plasma approaches, but advances in techniques and equipment design are narrowing the gap.

For our work, we opted for the well-established UV-YAG type laser system for two reasons: The laser industry has studied the feasibility of lasers extensively and has a strong data baseline, and our intent was to focus on microvia metallization after drilling, without adding a variable of laser types. Also, we had previously studied the characteristics of vias drilled with both laser types and possessed a functional understanding of pre-plating desmear and metallization relative to each laser system.

Typical Redistribution Dielectric Structures

A redistribution dielectric suitable with via drilling can be one of the following:

- FR-4 laminate, or prepreg with foil cap
- Resin coated foil
- Aramid laminate, or prepreg with foil cap
- Polyimide film-based laminate
- PTFE-based prepreg

A designer or fabricator's selection will in part depend on the via drilling approach. For example, inorganic reinforced materials will not plasma etch. Polyimide film is expensive, exhibits dimension stability sensitivity and is different chemically than the substrate, making processing difficult.

FR-4 and RCC are particularly attractive for several reasons: Their resin chemistries are similar to the substrate materials, which reduce problems with UL recognition, and their homogeneity facilitates fabrication steps. They are also the least expensive materials, and shops are quite familiar with their use.

RCC offers surface smoothness, thin dielectric, standard laminating steps, and ease of ablation due to its non-reinforced composition. FR-4 has not been widely acknowledged as suitable for redistribution layers because of its ablation characteristics were considered minimal with laser or plasma. The ability to add a sufficiently thin dielectric of high integrity (smoothness, uniformity, etc.) was also questioned. However, today many shops are able to lay up and laminate panels with 12 micron copper foil and one ply of FR-4 prepreg as thin as 1.7 mils. The laser suppliers have demonstrated the ability to drill vias through glass reinforced dielectrics at reasonable speed and integrity.

Based on the level of interest found in the industry for using RCC and FR-4 with lasers, and the corresponding need to understand the metallization processes required to fabricate circuitry of high reliability, a comparison of typical versions of these materials developed as a primary objective for our companies.

Metallization Procedures

Metallizing a Z-axis interconnect in the form of a blind microvia typically 6 mils in diameter and 2 mils deep is not routine. Several atypical issues require attention. The via drilling processes, especially lasers, leave resin residue in the cavity. The dead-end geometry prevents chemistry flow/agitation; any evolved gas will obstruct uniform coverage. Some redistribution dielectrics may not exhibit typical response to cleaning (desmear) and seed layer deposition.

These issues were addressed by studies of laser drilled vias in RCC processed with alkaline permanganate desmear and direct plating metallization.

Desmear

Work began with conventional permanganate parameters, including a solvent-based sensitizer and a high pH potassium permanganate etched. Weight loss testing was used, looking for a response of approximately 0.3 mg/cm^2, which is considered representative of sufficient desmear of most drilled holes.

FR-4 redistribution layers responded in typical fashion, and no special steps were required. Some RCC products on the other hand exhibited low weight loss; the high cross-linkage chemistry of the dielectric resin required some process refinement to reach an acceptable level of weight loss. Other RCC types are less chemically resistant and can be considered equivalent to FR-4 for process compatibility, although they also have lower Tg's which may not match up with the performance of the substrate material.

The following tables summarize evaluations of desmear processes on FR-4 and two types of coated foil, with weight loss based on the specific desmear process shown.

FR-4

Single Pass:		0.3-0.4 mg/cm2 wt. Loss
Hole Swell:	Commercially available or Butyl/Caustic	2 min/175°F
Permanganate:	80 g/l $KMnO_4$ 45 g/l NaOH	10 min/175°F
Neutralizer:	Commercially available	5 min/115°F

MultiFoil

Single Pass:		0.5-0.6 mg/cm^2
Hole Swell: Option A	Commercially available	0.3-0.4 mg/cm^2 2 min/175°F
Hole Swell: Option B	Butyl/Caustic	0.3-0.4 mg/cm^2 2 min/160°F
Permanganate:	80 g/l $KMnO_4$ 45 g/l NaOH	10 min/175°F
Neutralizer:	Commercially available	5 min/115°F

RCC

Single Pass:		0.1-0.12 mg/cm^2
Hole Swell:	Commercially available or Butyl/Caustic	5 min/175°F
Permanganate:	80 g/l $KmnO_4$ 45 g/l NaOH	15 min/175°F
Neutralizer:	Commercially available	5 min/115°F

Double Pass:		
Hole Swell: Option A	Commercially available	0.17-0.2 mg/cm^2 5 min/175°F
Hole Swell: Option B	Butyl/Caustic	0.2-0.25 mg/cm^2 5 min/160°F
Permanganate:	80g/l $KmnO_4$ 45 g/l NaOH	15 min/175°F
Neutralizer:	Commercially available	5 min/115°F

Single Pass:		0.2-0.25 mg/cm^2
Hole Swell:	Commercially available	5 min/175°F
Permanganate:	22% v/v $NaMnO_4$ 60 g/l NaOH	15 min/175°F
Neutralizer:	Commercially available	5 min/115°F

The above data quantifies responsivity to desmear in weight loss, along with a description of the permanganate chemistry. For RCC, acceptable results were found using conventional desmear chemistry: Single pass of sodium permanganate with commercially available hole swell.

The following photos provide evidence of the need for effective desmear in microvias.

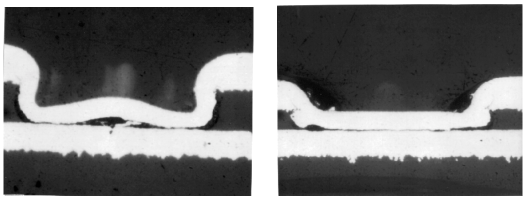


Figure 1: Photos of CO_2 laser vias with resin on target pad – not desmeared. Copper electroplated for 45 min at 25 ASF.

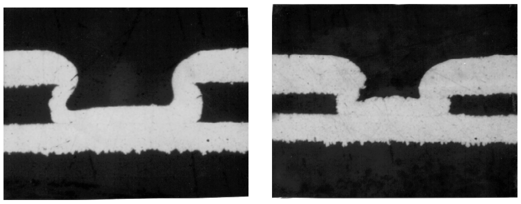


Figure 2: Photos of CO_2 laser vias with resin on target pad – desmeared. Copper electroplated for 45 min. at 25 ASF.

The following photos are FR-4 redistribution layers of approximately 3 mils thickness. A conventional desmear and glass etch provides noticeable improvements to the microvias features and the plating uniformity.

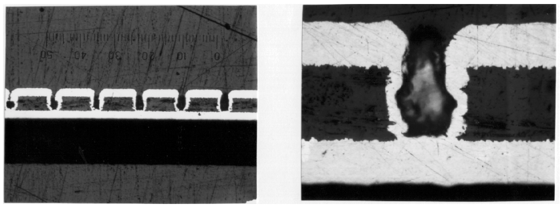
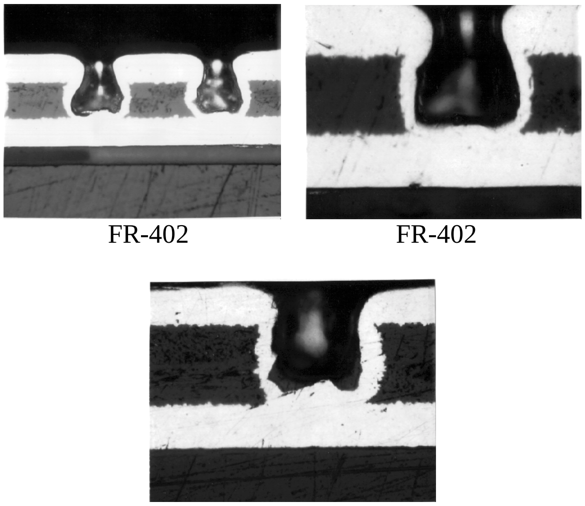


Figure 3: Photos of vias ablated with UV-YAG Laser and metallized with colloidal graphite copper electroplated for 60 min. at 25 ASF.
Material: FR-406-2X106
Thermal Stress: None
Desmear: None


FR-402 FR-402

FR-404

Figure 4: Photos of vias ablated with UV-YAG Laser and metallized with colloidal graphite copper electroplated for 60 min. at 25 ASF.
Material: FR-402 2x 106
FR-404 2 x 106
Thermal Stress: None
Desmear: Permanganate and Glass Etch
Cycle 2/10/5

Direct Plating

A direct plating approach was chosen early on, because conventional electroless was known by prior experience to have some limitations with small hole geometries. The colloidal graphite technology available from one of the team members became the primary metallization approach for our initial phase. The performance of this direct plating system appears to be well suited for blind microvia metallization, with good adhesion, complete coverage, and uniform deposition, while readily removable from panel surfaces of the panel. In particular, direct plating resulted in copper thickness in the via comparable with surface thickness, relative to that achieved with electroless.

Results of colloidal graphite plating studies are represented in the following table. Microsections of vias plated with colloidal graphite based direct metallization are compared with conventional electroless.

Colloidal Graphite Parameters for Conveyorized Process with Fixer

Chemical Steps	Process Temp. and Time
Cleaner/Conditioner	125-130°F 20-30 sec.
Rinse	Ambient 15-20 sec.
Colloidal Graphite	Ambient
1%-4% solids	30-40 sec.
**Fixer	80-120°F 10-15 sec.
**Rinse	Ambient 10-15 sec.
Dry	140-150°F 30-40 sec.
Microetch	Ambient 20-30 sec.
Rinse	Ambient 10-15 sec.
Antitarnish	Ambient 10-15 sec.
Rinse	Ambient 10-15 sec.
Dry	140-150°F 20-25 sec.
Output	

** Optional, depending on hole size

Electrolytic Copper Process Parameters for Colloidal Graphite and Electroless Copper

Chemical Step	Process Temp. and Time
Acid Cleaner, 10%	120-125°F 2.5-3.5 min.
Rinse	Ambient 1 min.
Microetch	Ambient 20-30 sec.
Rinse	Ambient 1 min.
Sulfuric Acid 10%	Ambient 1 min.
Acid Copper PC 667[1] or PC 606[1]	Ambient 15-75 min at 20-25 ASF
Rinse	Ambient 1 min.
Dry	140-150°F 4-5 min.

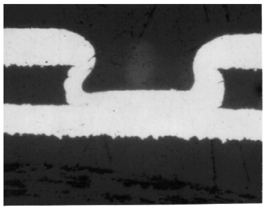


Figure 5: Photos of vias metallized with colloidal graphite with Fixer. Copper electroplated for 45 min. at 25 ASF.

---

[1] Acid copper from Electrochemicals, Inc.

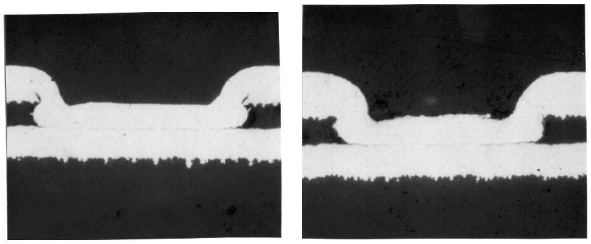


Figure 6: Photos of vias metallized with colloidal graphite without Fixer. Copper electroplated for 45 min. at 25 ASF.

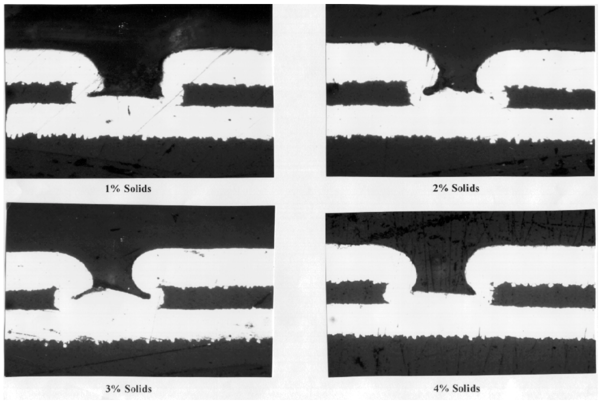


Figure 7: Photos of vias metallized with colloidal graphite at various solid concentrations with Fixer. Copper electroplated for 45 min. at 25 ASF.

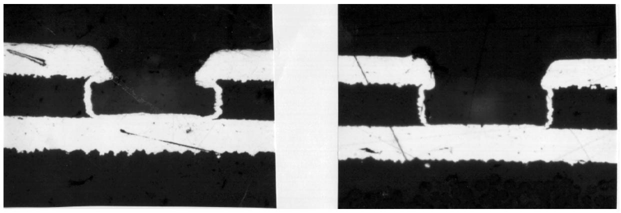


Figure 8: Photos of vias metallized with conventional electroless copper and electroplated for 45 min. at 25 ASF.

Evaluation of Plated Microvias by Microsection and Thermal Stress Testing

After completion of the work to understand the processes for via drilling and metallization in RCC and FR-4, studies of performance ensued. The first hurdle to clear was microsectioning -- to scrutinize the features of a six mil. diameter via requires considerable skill in section preparation. The photomicrographs attest to the skill base acquired through this work.

Thermal stress testing was used to look at structure integrity. Potential problems include weakness in the resin sidewall from improper desmear, blowholes, hole wall pullaway, etc. Coupons were subjected to 5x cycles of the standard 10 seconds float at 550°F. No prebake was used. Results showed no damage or apparent failure of the metallized vias.

Figures 9, 10, and 11, below, show microvias with direct plating and incrementally greater electroplating thicknesses. The microvias in Figure 9 and 10 were laser drilled, while the microvias in Figure 11 were formed with plasma. In each case, when plated at 45 and 70 minutes, the thicker copper resulted in no defects or degradation after the thermal stressing.

Microvia Thermal Stress Chart

Material	**Via Drilling**	**Cleaning**	**Metallization**	**Final Electroplating**		
				Brightner System	Current Density ASF	Time in min.
RCC	UV-YAG	Permanganate	Colloidal Graphite	PC 667[1]	20	15
MultiFoil	CO_2	Plasma	Electroless Copper	PC 606[1]	25	20
FR-4	Plasma					45
						75

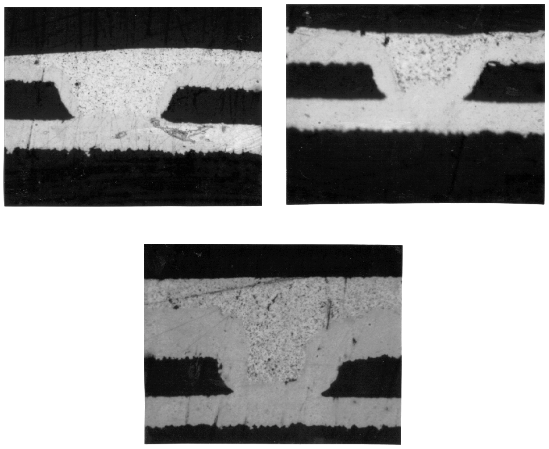


Figure 9: Photos of vias ablated with UV-YAG Laser and metallized with colloidal graphite copper electroplated for 20, 45 and 75 min. at 25 ASF.
Material: RCC-183525
Thermal Stress: 5 x 10 sec, 550°F
Desmear: Permanganate, cycle 5/15/5

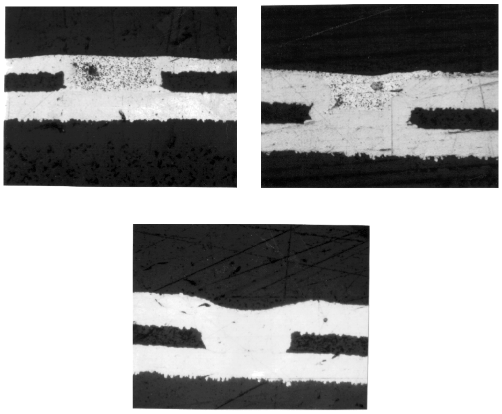


Figure 10: Photos of vias ablated with UV-YAG Laser and metallized with colloidal graphite. Copper plated for 15, 45 and 75 min. at 25 ASF.
Material: MultiFoil
Thermal Stress: 5 x 10 sec, 550°F
Desmear: Permanganate, cycle 2/5/5

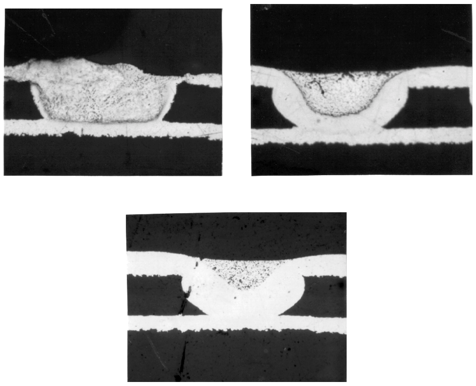


Figure 11: Photos of vias ablated on pre-etched copper targets with Isotropic Plasma and metallized with colloidal graphite copper electroplated for 15, 45 and 75 min. at 25 ASF.
Material: RCC
Thermal Stress: 5 x 10 sec, 550°F
Desmear: None

Multi Company Project to Assess Microvia Process Capability and Reliability

Electrochemicals, Hadco, and AlliedSignal Laminates agreed to a joint effort to demonstrate the current art of microvia fabrication, and determine the reliability of microvia interconnects by thermal cycling.

The plan included the following basic steps:

1. Selection of a test appropriate to the task of demonstrating microvia interconnect reliability under circumstances acceptable to the industry.

   The objective included a demonstration of whether production-derived plated microvias are capable of performance in thermal cycling equal to plated through vias. And if found comparable, to extend the measurement looking for the failure point, although not beyond normal expectations.

   The testing medium selected was IPC TM 2.6.26 (proposed), DC Current Induced thermal cycling test, commonly known as IST. This is a relatively new approach to reliability testing, which offers flexibility in coupon design and speed of test, while resulting in failures mechanisms that replicate the more conventional air-to-air testing.

2. Design a test coupon that represents the density and feature sets to be found in HDI/BUM boards. The final coupon incorporate both blind microvias and through vias; it also has two sizes of microvias and through vias. These parameters extend the data to capture a larger population of board features and potential sources of defects.

===================================

Coupon Feature	Target Size	
RCC dielectric thickness (nom)		50µ
FR-4 dielectric thickness (nom)		60µ
Thru via diameters	0.0135"	0.040”
Pad diameters (thru vias)	0.028"	0.054”
Blind microvias diameters	75µ	150µ
Pad diameter (capture pads)		0.012"
Grid pitch		0.100"
Plating thickness in thru vias		25µ
Plating thickness in microvias		[not controlled]

====================================

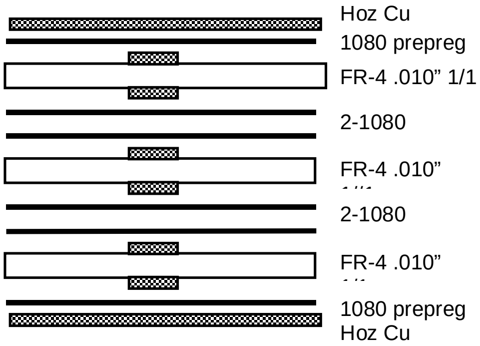
The features of the BUM test coupon and panel were selected to complement and build on the partners' expertise and experiences, keeping consistent with attainment of maximum benefits from the specified testing.

BUM Type A, Material Build

a. Layer count: 8 layers

b. Structure:
   - Innerlayers (2/3, 6/7): FR-4 0.010” Cu 1/1
   - Innerlayers (4/5): FR-4 0.010” Cu 1/1
   - Cap layers (1, 8): FR-4 1080 pp + Cu foil H oz
   - Bond layers: 2x FR-4 pp 1080

c. Overall thickness: 0.054±0.004”

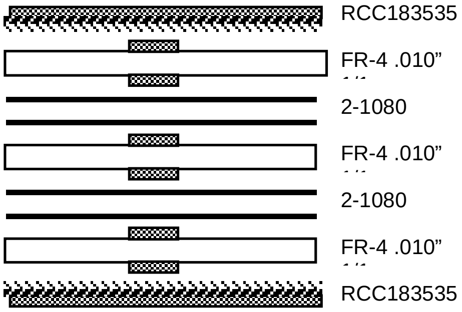


BUM Type B, Material Build

a. Layer count: 8 layers

b. Structure:
  - Innerlayers (2/3, 6/7): FR-4 0.010” Cu 1/1
  - Innerlayers (4/5): FR-4 0.010” Cu 1/1
  - Cap layers (1, 8): RCC183535 (resin coated foil)
  - Bond layers: 2x FR-4 pp 1080

c. Overall thickness: 0.054±0.004”



3. Conduct evaluations of the tested coupons and features, which locate failures and identify breakdown modes, needed to categorize and resolve root cause mechanics. The deliverables are expected to be a body of evidence that represents microvia structures, produced from widely available redistribution materials and using on-line fabrication processes, that will serve as an interconnect system with reliability as required by the end-equipment manufacturer.

Conclusion

Microvia structures are considered the lynchpin of High-Density Interconnect printed circuit technology. Selection of an HDI fabrication system is in the hands of the board manufacturer and the OEM designer. Our work is showing that microvias in RCC and FR-4 type redistribution layers can be fabricated using mainstream manufacturing processes and will demonstrate functional reliability as required in high performance electronic equipment.

This collaborative project is in-progress, with coupons in fabrication at Hadco Santa Clara at the time this paper was written. The authors expect that initial results of the IST thermal cycling will be available for presentation by the time of IPC Expo, Long Beach, and a final report can be available in the fall.

Acknowledgments

The authors wish to acknowledge and thank the partners in this work, and their respective companies:

Mason Hu, Hadco Inc, Santa Clara CA

Bill Birch, PWB Interconnect Solution, Ottawa Canada

References

“The Use of Direct Metallization in the Production of Laser and Plasma Drilled Microvias for BGA Applications”, Michael Carano, Frank Polakovic, and C Edwin Thorn, IPC Expo, April 1997.

RCC is Registered Trademark of AlliedSignal Inc.